1/22/appeal brief

IR-1677 (2-1984)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF APPEALS AND INTERFERENCES

2/13/03

In re Patent Application of
Zhijun Qu et al.
Serial No.: 09/329,156
Filed: June 9, 1999

New York, New York
Date: January 21, 2003
Group Art Unit: 2811
Examiner: S. Hu

For: DUAL EPITAXIAL LAYER FOR HIGH VOLTAGE VERTICAL CONDUCTION POWER MOSFET DEVICES

Assistant Commissioner of Patents and Trademarks
Washington, D.C. 20231

APPEAL BRIEF UNDER 37 C.F.R. §1.192

Sir:

This appeal is taken from the Examiner's final rejection dated May 21, 2002, in connection with the above-identified application. The Notice of Appeal was filed in the United States Patent and Trademark Office on August 21, 2002.

I. REAL PARTY IN INTEREST

The real party in interest is the assignee, International Rectifier Corporation.

II. RELATED APPEALS AND INTERFERENCES

The applicants, the assignee and the undersigned attorneys are not aware of any related appeals or interferences.

III. STATUS OF CLAIMS

Claims 1-4, and 9 stand rejected and are pending.

IV. STATUS OF AMENDMENTS

No amendments were filed after the final rejection.

V. SUMMARY OF INVENTION

In power switching devices, such as MOSFETs, the resistance of the device during forward conduction (on-resistance) and the ability of the device to withstand breakdown under reverse voltage condition (breakdown voltage) are two important factors. Due to the physics of such devices, the reduction in the on-resistance (a desirable result) often leads to the reduction in the breakdown voltage (an undesirable result). It is desirable to have MOSFET structures that exhibit both low on-resistance and high breakdown voltage.

Breakdown under reverse voltage conditions occurs when the electric field in the vicinity of a pn junction approaches a critical limit. Fig. 2 of the specification graphically shows the relationship between the strength of the electric field as a function of depth during reverse voltage condition. As stated in the specification, the area under the curve is proportional to the breakdown voltage. (Specification, page 3, line 31 - page 4, line 2.) The present invention is concerned with changing the shape of the curve shown by Fig. 2 so that the area under the curve is increased in order to improve the breakdown voltage.

According to the present invention, the junction receiving layer 11 of a prior art device (as shown by Figure 1) is replaced by a high resistivity layer 21 and a low resistivity layer 20. The low resistivity layer receives the base regions 12. (See Fig. 3)

As graphically shown by Figure 4, the addition of the low resistivity layer increases the slope of a portion of the electric field curve and thus increases the area under the same, which, in turn, increases the overall breakdown voltage of the device. It should be noted that the portion of the electric field curve that is changed corresponds to the thickness of the low resistivity layer 20 (the junction receiving layer). Because the breakdown voltage of the device is improved by the addition of the low resistivity layer, the thickness of the die can be reduced. (Specification, pate 5, lines 3-9). The reduction of the thickness of the die as well as the reduction in the resistivity of the junction receiving layer (low resistivity layer) 20 lead to the reduction in the on-resistance of the device, without effecting its breakdown voltage, thereby allowing for a good balance between the on-resistance and the breakdown voltage. By referring to the disclosure of the invention, one skilled

in the art learns that by adjusting the depth of the low resistivity layer, the proper balance between the on-resistance and the breakdown voltage of the device can be achieved.

VI. ISSUES

Whether claims 1-4 and 9 are obvious under 35 U.S.C. §103(a) over EP 0118921 (Akiyama) in view of U.S. Patent No. 5,521,410 (Yamamoto) or in view of U.S. Patent No. 6,207,993 (Ishimura et al.).

VII. GROUPING OF CLAIMS

Claims 1-4, and 9 stand or fall together.

VIII. ARGUMENT

Claim 1 is the only independent claim in the application.

Claim 1, and claims depending from claim 1, have been rejected as obvious under 35 U.S.C. §103(a) over Akiyama in view of Yamamoto and separately over Akiyama in view of Ishimura et al.

Claim 1 calls for, in combination with other limitations, a first layer (which relates to the high resistivity layer 21), a second layer (which relates to the low resistivity layer 20), and a plurality of diffusions (which relate to the base regions 12) each of which has "a depth that is less than the thickness of said second layer whereby each diffusion is wholly contained within said second layer." (See claim 1).

The Examiner has concluded that Akiyama teaches all of the limitations of claim 1 except for the base regions which have a depth that is less than the depth of the second layer. However, the Examiner has stated that the depth of the base regions can be reduced when lower on-resistance is desired as taught by Yamamoto and Ishimura et al.

It is respectfully submitted that Akiyama and Yamamoto and Akiyama and Ishimura cannot be combined to obtain the subject matter of claim 1 in that Akiyama requires the base regions to extend into a low conductivity region in order provide the device with the ability to withstand breakdown under the reverse voltage conditions. Therefore, Akiyama teaches away from having base regions which are wholly contained within a high conductivity region.

Akiyama teaches a vertical conduction MOSFET with a high resistivity layer 12, a low resistivity layer 13 disposed atop the high resistivity layer 12, and a plurality of base regions 3 which are formed to extend below the low resistivity layer 13 into the high resistivity layer 12. Akiyama, page 4, lines 4-15.

The reason for extending the base regions 3 into the high resistivity layer 12 is explained as follows:

> In FIG. 2, in the high resistivity drain region 12 and in the well regions 3, indicated with the dotted lines D are the limits of depletion layer that is produced when the PN junction between the source and drain of this vertical type MOSFET is reversely biased.
>
> That is to say, when a voltage is applied between the drain electrode and the source electrode, a reverse bias is created at the PN junction between the high resistivity drain region 12 and the well regions 3, thereby causing the depletion layers corresponding to each well regions 3 to expand and link up with each other and producing the situation shown in FIG. 2. Consequently, in this case the breakdown voltage is primarily determined in the lower parts of the well regions 3.

The on-resistance in a device according to Akiyama is lower due to the low resistivity layer 13. (Akiyama, page 10, lines 10-19.) In its background section, Akiyama, however, teaches that if the low resistivity regions are extended to below the base regions, the device's ability to withstand breakdown under the reverse bias condition is compromised.

> [W]hen the resistivity of the high resistivity drain region is reduced, a large electric field is produced at the junctions with the well regions 3, and the breakdown voltage between the source and the drain decreases. This causes the defect that there is a limit to how far the resistivity of this drain region 2 can be reduced. (Akiyama, page 2, lines 22-27.)

It is well known in the MOSFET art that, under the reverse voltage condition, electric field lines are heavily concentrated around the corners of the base regions. The increase in the electric field due to the decrease in the resistivity of the drain region often causes breakdown around the corners of the base region because that is where the electric field lines are concentrated. To

overcome this problem, while retaining the low resistivity obtained by higher concentration of dopants in the drain region by the addition of the low resistivity layer 13, Akiyama proposes extending the bottom of each base region; i.e., the portion that includes the corners, into the high resistivity layer 12, so that the depletion layers caused by the reverse voltage may expand and link up, rather than concentrate on the corners of the base regions to cause breakdown.

Given the fact that Akiyama teaches that reducing the resistivity of the drain region leads to the reduction of the ability of the device to withstand breakdown under the reverse voltage condition, and given Akiyama's solution, which is to make only part of the drain region of low resistance and extend the bottom portions of the base regions into the high resistance area to increase the breakdown voltage, one skilled in the art would be led away from designing a device which includes base regions that are wholly contained within a low resistivity region as called for by claim 1. Therefore, it would be erroneous to state that the device shown by Akiyama can be modified by the teachings of some other reference to include base regions that are wholly contained within a low resistivity layer when Akiyama quite clearly teaches extending the base regions into the low resistivity region in order to overcome the problem associated with decreasing the resistivity of the area surrounding the base regions (particularly the bottom portions of the base regions), namely, unacceptably low breakdown voltage.

In addition, the subject matter of claim 1 cannot be obtained even if Akiyama and Yamamoto are combined. The Examiner has stated that the combination of the teachings of Akiyama and Yamamoto results in the subject matter of claim 1 because Yamamoto teaches that on-resistance may be improved if the depth of the base layer is reduced as allegedly can be deduced from "the correlation between the base layer depth and the on-resistance shown in Figs. 2 and 4". (Final Office Action, page 3, lines 10-13.) It is not clear how the reduction of the thickness of the base regions is relevant to the subject matter of claim 1. Claim 1 requires the base regions to be wholly contained within the low resistivity layer. There is no requirement bearing on the thickness of the base regions.

It is presumed that the Examiner has taken the position that if one follows the teaching of Yamamoto, one might make the base regions of low enough depth so that they may end up being "wholly contained" within the low resistivity layer. If in fact this is the Examiner's position, it is respectfully submitted that the Examiner, at most, is stating that Yamamoto contains a suggestion

to experiment in that there is no specific teaching in Yamamoto directing one skilled in the art to form the base regions only deep enough to contain the same within the low resistivity layer.

Furthermore, even if Akiyama and Yamamoto are combined, the subject matter of claim 1 is not obtained in that Akiyama teaches that the base regions must extend into the high resistivity layer. Thus, even if the teaching of Yamamoto is applied and the base regions are made less deep, according to the teaching of Akiyama the base regions must be at least deep enough to extend into the high resistivity region. Therefore, the combination of Akiyama and Yamamoto does not result in a device which includes base regions wholly contained within a low resistivity layer.

Regarding the rejection of claim 1 based on the combination of Akiyama and Ishimura et al., it is respectfully submitted that one skilled in the art would not be directed to use the teachings of Ishimura et al. to modify the device shown by Akiyama to obtain a device according to claim 1 because Ishimura et al. teaches that containing the base regions within a low resistivity layer leads to undesirable results.

The Examiner has stated that the combination of Akiyama and Ishimura et al. results in the subject matter of claim1 because Ishimura et al. teach base regions 3 that are not deep enough to extend to the high resistivity layer 2. According to the Examiner "it would have been obvious to one skilled in the art at the time the invention was made to make the semiconductor device of Akiyama with p-type diffusions being shallower than the second layer, so that a device with lowered on-resistance would be obtained". (Final Office Action, page 3, lines 14-17.)

In addition to base regions 3, Ishimura et al. teaches the diffusions 11A which extend into the high resistivity region 2. Ishimura et al. explains the reasons for providing the diffusions 11A as follows:

> In the power MOSFET of FIG. 1, the p^+(p) diffusion region 11A is disposed away from the p-type diffusion region 3 while being connected to the source electrode 8, and the lower portion 11Aa of the p^+(p) diffusion region 11A is located deeper than the lower portion 3a of the p-type diffusion region 3. Therefore, the semiconductor layer 100 is thinner beneath the p^+(p) diffusion region 11A which the fourth semiconductor region than beneath the p-type diffusion region 3 which is the first semiconductor region, and the avalanche current which is produced when an avalanche breakdown occurs in the power MOSFET flows into the p-type (p) diffusion

region 11A. This means that the avalanche current flows away from the parasitic npn transistor consisting of the n^+ diffusion region 12, the p-type diffusion region 3 and the n^+ source region 4, and in other words, this reduces the avalanche current flowing into the parasitic npn transistor, resulting in improvement in withstand avalanche voltage.

Since the n^+ semiconductor region 12 is formed beneath the lower portion 3a of the p-type diffusion region 3, the power MOSFET of the first preferred embodiment has an on-resistance lower than the prior-art one. As discussed with reference to FIGS. 21 to 23, providing a region of low resistance like the n^+ semiconductor region 12 beneath the lower portion 3a of the p-type diffusion region 3 reduces on-resistance because a portion of high current density exists also beneath the lower portion 3a of the p-type diffusion region 3.

Further, since no n^+ diffusion region 12 is disposed beneath the lower portion 11a of the $p^+(p)$ diffusion region 11A, it is possible to suppress reduction of the withstand avalanche voltage and the main withstand voltage as compared with the prior art. Col. 10, line 60 - col. 11, line 25. (Emphasis added.)

Ishimura et al. states that disposing the base regions in a low resistivity region reduces on-resistance. This concept, however, is not new. As stated above, Akiyama also states that reduction of the resistivity of the drain region reduces on-resistance.

The technical problem is not just reducing on-resistance. Rather, it is reducing on-resistance, while maintaining breakdown voltage at an acceptable level. Ishimura et al. recognizes the problem associated with the reduction of the breakdown voltage when the base regions are wholly contained within the low resistivity region and proposes regions 11A which extend into the high resistivity region in order to divert current from the base regions and thus reduce the risk of breakdown. It is important, therefore, to recognize that Ishimura et al. teaches that disposing the base regions within a low resistivity layer is undesirable, and proposes including regions such as regions 11A in order to overcome the problem associated with including base regions wholly within a low resistivity layer. Therefore, one skilled in the art would not be directed by Ishimura et al. to modify Akiyama to include base regions that are wholly contained within a low resistivity layer in that such a modification without more (such as addition of regions 11A) would not achieve a desirable outcome; i.e., a power device with an acceptable on-resistance and breakdown voltage limit.

IX. CONCLUSION

For the reason set forth above the rejection of the application should be reversed.

Our check No. 14860, which includes the amount of $320 to cover the appeal brief is attached hereto. This brief is being submitted in triplicate in accordance with 37 C.F.R. 1.192 and applicant reserves the right to request an oral hearing upon receipt of the Examiner's Answer.

If this communication is being filed after a shortened statutory time period has elapsed and no separate Petition is enclosed, the Commissioner of Patents and Trademarks is petitioned, under 37 C.F.R. §1.136(a), to extend the time for filing the required papers by the number of months which will avoid abandonment under 37 C.F.R §1.135. The fee under 37 C.F.R. §1.17 should be charged to our Deposit Account No. 15-0700.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on January 21, 2003

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Respectfully submitted,

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APPENDIX OF CLAIMS ON APPEAL

1. A semiconductor device comprising, in combination, a silicon substrate having a first and second surface; a first layer disposed on said first surface and having impurities of the n or p conductivity type uniformly distributed throughout the volume of said first layer; a second layer disposed on said first layer; said second layer having impurities of the same type as those in said first layer uniformly distributed therethrough and having a substantially uniform resistivity; the concentration of impurities in said second layer being greater than the concentration of impurities in said first layer; and a plurality of diffusions of a conductivity type opposite to that of said second layer distributed uniformly into the surface of said second layer and defining p-n junctions therein; said plurality of diffusions being spaced from one another and each having a depth that is less than the thickness of said second layer whereby each diffusion is wholly contained within said second layer.

2. The device of claim 1 wherein the resistivity of said second layer is lower than that of said first layer.

3. The device of claim 1 wherein the thickness of said first layer is greater than that of said second layer.

4. The device of claim 2 wherein the thickness of said first layer is greater than that of said second layer.

9. The device of claim 8 wherein said device is a vertical conduction power MOSFET.